Registration No: | | | | | | | | | | |

Total Number of Pages: 03 **MCA**

MCA102

1st Semester Regular Examination 2016-17
Computer Organization and Architecture
BRANCH: MCA
Time: 3 Hours
Max Marks: 100
Q.CODE: Y568

Answer Part-A which is compulsory and any four from Part-B.
The figures in the right hand margin indicate marks.

Part – A (Answer all the questions)

Q1 Answer the following questions: **(2 x 10)**

a) In a logical circuit there are 'n' binary inputs. The number of different input combinations in the truth table is
(a) 2n (b) 2/n (c) 2^n (d) 2(n+1)

b) Arithmetic logic unit
I. perform arithmetic operations
II. store data
III. perform comparison
IV. communicate with input devices
Out of the above the correct one is
(a) I only
(b) II only
(c) I and II only
(d) I and III only

c) How number systems are generally classified?
(a) Conditional or non-conditional
(b) Positional or non-positional
(c) Real or imaginary
(d) Literal or numerical

d) The duration between the read and the MFC signal and the minimum time delay between two successive memories read operations are _____ and _____ respectively.
(a) Access time and cycle time
(b) Latency and delay
(c) Cycle time and access time
(d) None of the above

e) A memory organization that can hold up to 1024 bits and has a minimum of 10 address lines can be organized into _____.
(a) 128 X 8
(b) 256 X 4
(c) 512 X 2
(d) 1024 X 1

f) The advantage of I/O mapped devices to memory mapped is
(a) The former offers faster transfer of data
(b) The devices connected using I/O mapping have a bigger buffer space
(c) The devices have to deal with fewer address lines
(d) No advantage as such

g) The transmission on the asynchronous BUS is also called as _____.
(a) Switch mode transmission
(b) Variable transfer
(c) Bulk transfer
(d) Hand-Shake transmission

h) In 8085 microprocessor, write the name of the 16 bit registers?
(a) Stack pointer
(b) Program counter
(c) a & b
(d) None of these

i) The cache usually gets its data from the_____ whenever the instruction or data is required by the CPU.
(a) Main memory
(b) Virtual memory
(c) Cache memory
(d) All of these

j) The no of interrupt lines used in 8085 microprocessor is
(a) 2 (b) 5 (c) 4 (d) 3

Q2 Briefly answer the following questions: **(2 x 10)**

a) Which gates are called as the universal gates? What are its advantages?

b) Justify the statement: "Irrespective of big endian or little endian, addresses of successive words in memory remain the same".

c) Differentiate between word addressing and byte addressing.

d) What is the importance of virtual memory and what is virtual address?

e) What is the difference between static RAM and dynamic RAM? Out of these which one is used in cache memory and why?

f) What is the difference between synchronous and asynchronous data transfer?

g) Differentiate between write back and write through protocol.

h) Explain the register indirect addressing scheme with suitable example

i) A cache has a 95% hit ratio, an access time of 100ns on a cache hit, and an access time of 800ns on a cache misses. Compute the effective access time.

j) What is the function of DAA instruction in 8085 microprocessor? Explain with a suitable example.

Part – B (Answer any four questions)

Q3 **a)** Explain the working principle of hardwired control unit and micro-programmed control unit with neat diagram. Write the advantages and disadvantages of both control units. **(10)**

b) Describe Von Neumann architecture with suitable block diagram. **(5)**

Q4 **a)** The following two signed numbers (negative numbers are represented using 2's compliment form) are given. Find their product using Booth's algorithm. **(8)**

A = (11011101), B = (11010111).

b) Consider a practical sized standard format of 12-bits for representation of floating point numbers, A and B that retains all pertinent concepts analogous to 32-bit IEEE format. **(7)**

A =	0	0111	101010
B =	0	10001	011011

i) Represent the numbers +19 in this format.
ii) Perform addition operation in the operands

Q5 **a)** What is the concept of direct memory access? Draw the block diagram of a DMA controller and explain how the data transfer takes place with the help of DMA. **(10)**

b) Define paging? Explain its working principle with a suitable example. **(5)**

Q6 **a)** State the functions of I/O module and explain the input/output subsystems with neat diagram. **(10)**

b) Differentiate memory mapped I/O and I/O mapped I/O. Write the advantages and disadvantages of both techniques. **(5)**

Q7 **a)** What do you mean by set associative mapping? With a neat diagram, explain its working principle. **(8)**

b) A memory system has 512K words each of 16-bits. The block size of cache is given as 4 words. Find out the number of bits in the TAG, BLOCK and WORD fields of a main memory address assuming that the mapping techniques is direct mapping. The cache memory has 2K words and it is word addressable. **(7)**

Q8 **a)** Write short notes on the following: **(10)**
i) Array Processors
ii) RISC versus CISC.

b) Briefly explain Flynn's Classification of computer architecture. **(5)**

Q9 **a)** Explain the pin diagram of 8085 microprocessor with neat diagram. Explain the direct addressing modes and indirect addressing modes of 8085 with example. **(10)**

b) Write a Program to Perform the following functions and verify the output. Steps are **(5)**
(a) Load the number 5CH in register D
(b) Load the number 9EH in register C.
(c) Increment the Contents of register C by one.
(d) Add the contents of register C and D and Display the sum.